Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A circuit for protecting the values stored in a BISR repair block in an integrated circuit having a custom test flow, comprising:

a plurality of soft latches within the BISR repair block, the soft latches being coupled together to form a BISR scan chain for holding BISR repair information; ~~and~~

means for providing a chip level scan enable signal for enabling a scan test, and a scan hold control signal for controlling holding of the repair information in the soft latches of the BISR scan chain,

wherein the chip level scan enable signal and the scan hold control signal cooperate to control connection of the BISR scan chain to other scan chains during a scan test, so that the BISR repair information is held within the soft latches and said scan test is any part of said custom test flow employing a BISR circuit[[.]];

means for providing a BISR scan signal suitable for causing the scan test to be run;

means for providing a diagnose enable signal, the diagnose enable signal cooperating with the chip level scan enable signal and the scan hold control signal for enabling debugging of logic connecting the BISR scan chains; and

means for receiving the chip level scan enable signal, the scan hold control signal, the BISR scan signal and the diagnose enable signal and providing a test enable signal and providing test enable signal determined by the expression

$$TE = BS \cdot \overline{DE} \cdot \overline{CLSE} \cdot \overline{SHC} + DE \cdot \overline{CLSE} \cdot \overline{SHC}$$

wherein TE is the test enable signal, BS is the BISR scan signal, DE is the diagnose enable signal, CLSE is the chip level scan enable signal, and SHC is the scan hold control signal.

2. (Original) The circuit as claimed in claim 1, wherein the chip level scan enable signal and the scan hold control signal cooperate to prevent the BISR scan chain from being connected to other scan chains.

3. (Cancelled)

4. (Cancelled)

5. (Original) The circuit as claimed in claim [[4]] 1, wherein the chip level scan enable signal, the scan hold control signal, the diagnose enable signal and the BISR scan signal are combined to provide a test enable signal for controlling connection of the BISR scan chain to other scan chains during a scan test.

6. (Cancelled)

7. (Original) The circuit as claimed in claim 3, wherein the BISR scan chain is connected in a single scan chain separate from logic forming other scan chains, and wherein the BISR scan chain is activated when required.

8. (Original) The circuit as claimed in claim 3, wherein the BISR scan chain is multiplexed with a normal scan chain.

9. (Original) The circuit as claimed in claim 8, wherein when the diagnose enable signal is low the BISR scan chain is bypassed by the scan test and wherein when the diagnose enable signal is high, the BISR scan chain is put

in the scan test path.

10. (Currently Amended) A method for protecting the values stored in a BISR repair block in an integrated circuit having a custom test flow, comprising:

storing repair information in a plurality of soft latches within the BISR repair block, the soft latches being coupled together to form a BISR scan chain for holding the BISR repair information; ~~and~~

providing a chip level scan enable signal for enabling a scan test and a scan hold control signal for controlling holding of the repair information in the soft latches of the BISR scan chain,

wherein the chip level scan enable signal and the scan hold control signal cooperate to control connection of the BISR scan chain to other scan chains during a scan test, so that the BISR repair information is held within the soft latches and said scan test is any part of said custom test flow employing BISR circuit[[.]];

providing a BISR scan signal suitable for causing the scan test to be run;

providing a diagnose enable signal, the diagnose enable signal cooperating with the chip level scan enable signal and the scan hold control signal for enabling debugging of logic connecting the BISR scan chains;

receiving the chip level scan enable signal, the scan hold control signal, the BISR scan signal and the diagnose enable signal; and

providing a test enable signal,

wherein the chip level scan enable signal, the scan hold control signal, the diagnose enable signal and the BISR scan signal are combined to provide the test enable signal for controlling connection of the BISR scan chain to other scan chains during a scan test.

11. (Original) The method as claimed in claim 10, wherein the chip level scan enable signal and the scan hold control signal cooperate to prevent the BISR scan chain from being connected to other scan chains.

12. (Cancelled)

13. (Cancelled)

14. (Cancelled)

15. (Original) The method as claimed in claim ~~14~~ 10, wherein the test enable signal is determined by the expression

$$TE = BS \times DE \times \overline{CLSE}.X\ SHC + \overline{DE} \times CLSE.X\ SHC$$

wherein TE is the test enable signal, BS is the BISR scan signal, DE is the diagnose enable signal, CLSE is the chip level scan enable signal, and SHC is the scan hold control signal.

16. (Original) The method as claimed in claim 15, wherein the scan hold control signal and the diagnose enable signal are provided by a TAP controller.

17. (Original) The circuit as claimed in claim 12, wherein the BISR scan chain is connected in a single scan chain separate from logic forming other scan chains, and wherein the BISR scan chain is activated when required.

18. (Original) The circuit as claimed in claim 12, wherein the BISR scan chain is multiplexed with a normal scan chain.

19. (Original) The circuit as claimed in claim 18, wherein when the diagnose enable signal is low the BISR scan chain is bypassed by the scan test and wherein when the diagnose enable signal is high, the BISR scan chain is put in the scan test path.

20. (Currently Amended) A memory employing a Built In Self Repair circuit and having a scan test as a part of a custom test flow, comprising:

a circuit for protecting the values stored in a BISR repair block, including:

an array of memory elements;

a BISR circuit for providing testing and soft repair of a memory element within the array;

a plurality of soft latches controlled by the BISR circuit, the soft latches being coupled together to form a BISR scan chain for holding BISR repair information; and

~~means for providing a chip level scan enable signal for enabling a scan test and a scan hold control signal for controlling holding of the repair information in the soft latches of the BISR scan chain,~~

circuitry for providing a test enable signal, comprising:

a chip level scan enable pin for a signal enabling a scan test,

a scan hold control pin for a signal controlling holding of the repair information in the soft latches of the BISR scan chain,

a BISR scan pin for a BISR scan signal suitable for causing the scan test to be run and

a diagnose enable pin for a diagnose enable signal for enabling debugging of logic connecting the BISR scan chains,

wherein the signal enabling a scan test and the signal controlling holding of the repair information ~~the chip level scan enable signal and the scan hold control signal~~ cooperate to control connection of the BISR scan chain to other scan chains during a scan test~~, so that~~ whereby the BISR repair information is held within the soft latches.

21. (Original) The memory as claimed in claim 20, wherein the chip level scan enable signal and the scan hold control signal cooperate to prevent the BISR scan chain from be connected with other scan chains.

22. (Currently Amended) The memory as claimed in claim 20, ~~further~~

~~comprising means for providing a diagnose enable signal,~~ wherein the diagnose enable signal cooperates ~~cooperating~~ with the chip level scan enable signal and the scan hold control signal for enabling debugging of logic connecting the BISR scan chains.

23. (Cancelled)

24. (Currently Amended) The memory as claimed in claim ~~23~~ 20, wherein the chip level scan enable signal, the scan hold control signal, the diagnose enable signal and the BISR scan signal are combined to provide a test enable signal for controlling connection of the BISR scan chain to other scan chains during a scan test.

25. (Original) The memory as claimed in claim 24, wherein the test enable signal may be determined by the expression

$$TE = BS \cdot DE \cdot \overline{CLSE} \cdot SHC + DE \cdot CLSE \cdot \overline{SHC}$$

wherein TE is the test enable signal, BS is the BISR scan signal, DE is the diagnose enable signal, CLSE is the chip level scan enable signal, and SHC is the scan hold control signal.

26. (Currently Amended) The memory ~~circuit~~ as claimed in claim 22, wherein the BISR scan chain is connected in a single scan chain separate from logic forming other scan chains, and wherein the BISR scan chain is activated when required.

27. (Currently Amended) The memory ~~circuit~~ as claimed in claim 22, wherein the BISR scan chain is multiplexed with a normal scan chain.

28. (Currently Amended) The memory ~~circuit~~ as claimed in claim 27,

wherein when the diagnose enable signal is low the BISR scan chain is bypassed by the scan test and wherein when the diagnose enable signal is high, the BISR scan chain is put in the scan test path.

29. (New) A memory employing a Built In Self Repair circuit and having a scan test as a part of a custom test flow, comprising:

a circuit for protecting the values stored in a BISR repair block, including:

an array of memory elements;

a BISR circuit for providing testing and soft repair of a memory element within the array;

a plurality of soft latches controlled by the BISR circuit, the soft latches being coupled together to form a BISR scan chain for holding BISR repair information; and

circuitry for providing a test enable signal, including:

a chip level scan enable pin for receiving a signal enabling a scan test,

a scan hold control pin for receiving a signal controlling holding of the repair information in the soft latches of the BISR scan chain,

a BISR scan pin for receiving a BISR scan signal suitable for causing the scan test to be run and

a diagnose enable pin for receiving a diagnose enable signal for enabling debugging of logic connecting the BISR scan chains,

wherein the test enable signal being determined by the expression

$$TE = BS \cdot DE \cdot CLSE \cdot SHC + \overline{DE} \cdot \overline{CLSE} \cdot SHC$$

wherein TE is the test enable signal, BS is the BISR scan signal, DE is the diagnose enable signal, CLSE is the chip level scan enable signal, and SHC is the scan hold control signal.

30. (New) The memory as described in Claim 29, wherein the chip level

scan enable signal and the scan hold control signal cooperate to control connection of the BISR scan chain to other scan chains during a scan test, so that the BISR repair information is held within the soft latches.

31. (New) The memory as claimed in claim 29, wherein the BISR scan chain is connected in a single scan chain separate from logic forming other scan chains, and wherein the BISR scan chain is activated when required.

32. (New) A method for protecting the values stored in a BISR repair block in an integrated circuit having a custom test flow, comprising:

storing repair information in a plurality of soft latches within the BISR repair block, the soft latches being coupled together to form a BISR scan chain for holding the BISR repair information;

providing a chip level scan enable signal for enabling a scan test;

providing a scan hold control signal for controlling holding of the repair information in the soft latches of the BISR scan chain;

providing a BISR scan signal suitable for causing the scan test to be run;

providing a diagnose enable signal, the diagnose enable signal cooperating with the chip level scan enable signal and the scan hold control signal for enabling debugging of logic connecting the BISR scan chains;

providing a test enable signal, wherein the chip level scan enable signal, the scan hold control signal, the diagnose enable signal and the BISR scan signal are combined to provide a test enable signal for controlling connection of the BISR scan chain to other scan chains during a scan test.

33. (New) The method as described in Claim 32, wherein the chip level scan enable signal and the scan hold control signal cooperate to control connection of the BISR scan chain to other scan chains during a scan test whereby

the BISR repair information is held within the soft latches and said scan test is any part of said custom test flow employing BISR circuit.

34. (New) The method as claimed in claim 32, wherein the chip level scan enable signal and the scan hold control signal cooperate to prevent the BISR scan chain from being connected to other scan chains.

35. (New) The circuit as claimed in claim 32, wherein the BISR scan chain is connected in a single scan chain separate from logic forming other scan chains, and wherein the BISR scan chain is activated when required.

36. (New) The method as claimed in claim 32, wherein the test enable signal is determined by the expression

$$TE = BS \cdot \overline{DE} \cdot \overline{CLSE} \cdot SHC + DE \cdot CLSE \cdot SHC$$

wherein TE is the test enable signal, BS is the BISR scan signal, DE is the diagnose enable signal, CLSE is the chip level scan enable signal, and SHC is the scan hold control signal.

37. (New) The method as claimed in claim 32, wherein when the diagnose enable signal is low the BISR scan chain is bypassed by the scan test and wherein when the diagnose enable signal is high, the BISR scan chain is put in the scan test path.